

**ADAPTIVE METHOD AND APPARATUS TO CONTROL LOOP BANDWIDTH  
OF A PHASE LOCK LOOP**

TECHNICAL FIELD

5       The invention relates to adaptive control of the loop bandwidth of a PLL (Phase Lock Loop).

BACKGROUND

10       In the majority of PLL systems, there is an inherent tradeoff between reducing 'lock in time' and jitter that results from noise in the reference signal. A narrow band width attenuates small noise from the reference/input signal, thereby resulting in reduced noise and induced jitter at the output. However, reduced bandwidth implies an increase in

15       lock-in-time of the PLL. There have been many approaches used to reducing lock-in-time of PLLs. These include digital/DSP (Digital Signal Processing) methods, dual loop/PLL architectures, feed forward compensation techniques, and variable loop bandwidth methods. In the DSP method, the phase

20       error is fed in to a 'fast DSP processor' whose output is then used to adjust the center operating frequency of a VCO (Voltage Controlled Oscillator). Once the error is reduced below some threshold, the VCO voltage from the DSP will be fixed and the PLL loop will take over. In the dual loop/PLL

25       approach, the first loop is used to accomplish a channel select. Since the desired channel is externally selected, the first loop will then quickly lock-in to the desired channel. This channel is then fed to the second PLL loop. In the feed forward method, an estimate of the frequency of the

30       input/reference clock is made which is then used to set the

VCO center frequency. Once this is done, the PLL loop can take over. By far the most common approach to reducing lock-in-time involves changing loop parameters. In particular, it involves varying the filter time constants to vary the loop bandwidth. There are also various complicated or otherwise unwieldy techniques for adaptively changing loop bandwidth parameters.

It would be desirable to provide a relatively simple and straightforward approach to varying the loop bandwidth.

#### SUMMARY OF THE INVENTION

The present invention comprises using a "feed forward" signal in combination with a switched-capacitor to effect a variation in loop bandwidth of a PLL.

#### BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and its advantages, reference will now be made in the following Detailed Description to the accompanying drawings, in which:

FIGURE 1 is a block diagram of a typical prior art PLL;

FIGURE 2 is a circuit diagram of a simplified switched capacitor circuit;

FIGURE 3 comprises a set of waveforms used in explaining the use of FIGURE 2 in providing a variable impedance in FIGURE 4;

FIGURE 4 is a combined circuit/block diagram of a PLL;

FIGURE 5 is a graph illustrating normalized PLL bandwidth versus frequency error;

FIGURE 6 is an implementation of R3 of FIG. 3;

FIGURE 7 illustrates a plot of a frequency response at a node N in FIGURE 4;

FIGURE 8 illustrates voltage/current characteristics for a switched capacitor resistor which is connected to node N, wherein the  $V_{in}$  applied to the switched capacitor resistor corresponds to the voltage at node N, and  $V_{ref}$ =ground; and

FIGURE 9 illustrates voltage/current characteristics for a switched capacitor resistor which is connected to node N wherein  $V_{in}$  to the switched capacitor resistor corresponds to the voltage at node N, and  $V_{ref}$  is less than ground.

#### DETAILED DESCRIPTION

In the following discussion, numerous specific details are set forth to provide a thorough understanding of the present invention. However, those skilled in the art will appreciate that the present invention may be practiced without such specific details. In other instances, well-known elements have been illustrated in schematic or block diagram form in order not to obscure the present invention with unnecessary detail.

In FIGURE 1, a reference clock signal is applied on a lead 10 to a first input of a PFD (Phase/Frequency Detector) 12. An LPF (Low Pass Filter) 14 is connected between an output of PFD 12 and an input of a VCO (Voltage Controlled Oscillator) 16. Although not required, the frequency of an output signal at an output lead 18 of the VCO is a multiple (or sub multiple) of the reference frequency signal applied on lead 10. Thus a frequency divider or adjuster 20 is used to revise the frequency of the signal on lead 18 to a frequency which is the same as the reference frequency when the PLL

(Phase Lock Loop) circuit of FIGURE 1 is in a locked condition. This adjusted frequency appears at the output of block 20 on a lead 22 which provides a feedback clock second input to PFD 12.

5        Within LPF 14, there is typically a resistance shown as resistor 24 which is also designated as R1. Resistor 24 is connected between an input of the LPF and an output lead 26 of the LPF. A capacitor 28 is connected in series with a resistance 30 between lead 26 and a ground connection 32.  
10    Capacitor 28 is further designated  $C_{\text{filter}}$  and resistor 30 is further designated as R2. Resistor 30 is often referred to in the art as a damping resistor.

FIGURE 2 illustrates a basic switched capacitor circuit. As shown, a capacitor 50 is connected between a common lead of  
15    a switch 52 and ground 54. One terminal 56, of switch 52, is connected to a source of energy, such as a battery source, while another terminal 58 is connected to a reference potential or ground. For purposes of discussion, a lead connected to terminal 56 is labeled  $V_{\text{in}}$  and  $I_{\text{in}}$  thereby  
20    indicating an applied voltage and resulting current. A dash line 60, which is also labeled  $V_{\text{switch}}$ , is used to represent a switching action of switch 52 between contacts or terminals 56 and 58 to charge capacitor 50 in one position and discharge it in the other position.

25        A plurality of signal waveforms are presented in FIGURE 3. A first waveform is representative of a switching signal of a given frequency that might be applied to the switch of FIGURES 2 or 4. Waveform 300 is shown to have a period of "T" for one cycle of operation. A waveform 302 is representative  
30    of the substantially constant voltage that would appear at

terminal 56 of the switch 52 or at the point Node N of FIGURE 4. Waveform 304 is representative of the voltage appearing across the plates of capacitor 50 with the constant voltage  $V_{in}$  applied to terminal 56 of FIGURE 2. Similarly, a waveform 306 is representative of the current flowing into capacitor 50 as a result of the action of switching signal 300 and the applied voltage  $V_{in}$ . Waveforms 304 and 306 are further designated as  $V_c$  (or  $V_{capacitor}$ ) and  $I_{in}$ , respectively. Finally, a waveform 308 is representative of the current flowing into capacitor 50 from terminal 56 and out of capacitor 50 to terminal 58 and to ground 54. As the frequency of the switch signal 300 decreases, the current  $I_{in}$  decreases in total amount, thereby increasing the effective resistance as presented infra in connection with formulas presented in the technical discussion.

In FIGURE 4, a reference clock signal is applied on a lead 402 to a first input of a PFD 404. An LPF 406 is connected between an output of PFD 404 and an input of a VCO 408. Again, the frequency of an output signal at an output lead 410 of the VCO 408 is a multiple (or sub multiple) of the reference frequency signal applied on lead 402. Thus, a frequency divider or adjuster 412 is used to revise the frequency of the signal on lead 410 to a frequency which is the same as the reference frequency when the PLL (Phase Lock Loop) circuit is in a stable and locked condition. This adjusted frequency appears at the output of block 412 on a lead 414 which provides a feedback clock second input to PFD 404.

Thus far, FIGURE 4 is similar to the prior art FIGURE 1. However, in FIG. 4, a frequency mixer or difference signal

generating means 416 is used to mix received signals at frequencies  $W_{\text{feedback}}$  and  $W_{\text{ref}}$  from adjuster 412 and reference input 402, respectively. An output signal  $W_{\text{ref}} - W_{\text{feedback}}$  from mixer 416 is provided on a lead 418. This signal, with a frequency of  $W_{\text{ref}} - W_{\text{feedback}}$ , is of a frequency indicative of the difference between the reference frequency and the output of the VCO. In the locked state, the frequency of the output signal of mixer 416 reduces to zero. In other words, the output signal is a DC or close to DC value.

A further difference of FIGURE 4 over FIGURE 1 lies within LPF 406. As shown, an LPF input resistor 420 is connected between the output of PFD 404 and a lead 421 providing an output signal from LPF 406. Resistor 420 is further designated as R1. A filter capacitor 422 is connected in series with a damping resistor 424 between lead 421 and a ground connection 426. The capacitor 422 is further designated as  $C_{\text{filter}}$  while the damping resistor 424 is further designated as R2. A variable resistance or impedance 428 is connected in parallel with R2 424. The impedance of resistor 428 varies from substantially infinite to some much lower value as a function of the frequency of a signal applied on a  $V_{\text{switch}}$  lead 418. Although impedance 428 is shown as a variable resistor, this entity is implemented in the form of the switched capacitor of FIGURE 2.

As known to those skilled in the art, variable resistors have been previously implemented in integrated chip circuits in switched capacitor format. When the frequency of the switching signal to a switched capacitor is high, the resistance is low and when the frequency reduces to near zero, the resistance approaches an infinite value.

As previously mentioned, FIGURE 1 shows a typical prior art charge pump based PLL architecture. The LPF 14 is a simple RC type even though active filters can also be used. Assuming the LPF 14 operates in a regime such that the PFD 12 can be modeled as a continuous time machine with gain  $K_{pfd}$ , and assuming the VCO as a perfect integrator with gain  $K_{vco}$ , and for ease of calculation setting divider ratio, N equal to 1, we will arrive at the following loop equation (1):

$$\theta_{out}(w) / \theta_{in}(w) = (K + jwK\tau_2) / (K - w^2\tau_1 + jw(1 + K\tau_2)) \quad (1)$$

where  $K = K_{pfd}K_{vco}$ ,

$$\tau_1 = (R_1 + R_2)C_{filter}, \text{ and} \quad (2)$$

$$\tau_2 = R_2C_{filter} \quad (3)$$

$\theta_{out}$  is the phase of signal generated by the VCO and  $\theta_{in}$  is the phase of the reference clock.

The natural angular frequency, which also corresponds to the loop bandwidth, is given by equation (4):

$$\omega_n = K / \tau_1 \quad (4)$$

Therefore, to obtain a large bandwidth, it is appropriate to minimize  $\tau_1$  and/or maximize  $K$ .

Reference may now be made to the simplified switched

capacitor resistor circuit of FIGURE 2 along with the timing diagram waveforms of FIGURE 3. It may be assumed that  $V_{in}$  (FIG. 2) is quasi-stationary with respect to  $V_{switch}$ . This assumption is further explained infra. When  $V_{switch}$  is high, current is flowing into the capacitor 50 from  $V_{in}$ . This current  $I_{in}$ , taking into account the effect of finite switch resistance, is shown in FIG. 3 as waveform 304 for a  $V_{switch}$  frequency of that shown in waveform 300. When the potential of  $V_{switch}$  is low,  $V_{in}$  is disconnected from the capacitor 50 and capacitor 50 is discharged. This process is repeated in accordance with the frequency of the  $V_{switch}$  signal 300.

The average current that is extracted from  $V_{in}$  can be computed as follows. Assuming  $V_c$  (waveform 302) reached  $V_{in}$ , the total charge  $Q_{tot}$  deposited by  $V_{in}$  into capacitor C during the time when switch 58 (waveform 300) is ON is given by equation (5):

$$Q_{tot} = CV_{in} \quad (5)$$

20

In other words during each switch period (T), an amount of charge equal to  $CV_{in}$  is transferred from node  $V_{in}$  to the capacitor. Therefore the average current is then:

$$I_{av} = CV_{in}/T \quad (6)$$

25

The average resistance seen looking into node  $V_{in}$  is then:

$$R_{av} = V_{in}/I_{av} = 1/fC \quad \text{where } f = 1/T$$

30

(7)

Equation (6) is arrived at by assuming ideal switches.

Next,  $R_{av}$  may be derived for the case where the switches  
 5 exhibit finite resistance. In this case, the total amount of  
 charge transferred to the capacitor  $C$  is obtained by  
 integrating the instantaneous input current over the duration  
 of 0 to  $T/2$ .

10 The instantaneous current is given by:

$$I(t) = (V_{in}/R) e^{(-t/RC)}$$

(8)

15 where  $R$  is the switch ON resistance.

$Q_{tot} = \int I(t) dt$  where the integral limits are from  $t=0$  to  
 $t=T/2$

20 Expressed differently,

$$Q_{tot} = -V_{in}C[e^{(-T/(2RC))} - 1]$$

(9)

25  $I_{av}$  may be obtained by using the following equation:

$$I_{av}T = Q_{tot}$$

(10)

30  $R_{av}$  is given by (7).

Therefore:

$$R_{av} = -1 / (fC[e^{(-2f/RC)} - 1]) \text{ where } f=1/T$$

5 (11)

It may be noted, that, in the limit as R approaches zero, equation (11) reduces to (7)

FIGURE 4 shows a simple application of a variable  
10 impedance (the switched capacitor resistor of FIGURE 2) within a PLL to dynamically adjust loop bandwidth. For ease of argument, it may be assumed that R1 (420) is zero, the loop bandwidth is determined by K and the time constant  $\tau$ :

$$\tau = (R_2 // R_3) C_{filter}$$

15 (12)

where  $(R_2 // R_3)$  is the effective impedance of resistors 424 and 428 connected in parallel.

20 As previously noted, variable resistor 428 is actually a switched capacitor resistor like in FIGURE 2. The reference and feedback clocks on leads 402 ( $W_{ref}$ ) and 414 ( $W_{feedback}$ ), respectively, are 'mixed' using the mixer 416. The resulting signal with a fundamental frequency of  $W_{ref} - W_{feedback}$  is then  
25 used to control the value of the switched capacitor resistor. When the PLL of FIGURE 4 is significantly out of lock, that is when the difference frequency  $W_{ref} - W_{feedback}$  is large,  $R_3$  or resistance 428 is reduced. This directly results in increased loop bandwidth as set forth in equation 12. When the PLL  
30 achieves lock, that is, when  $W_{ref}$  and  $W_{feedback}$  are the same, the

mixer's output will be a dc signal corresponding with an infinite impedance in the leg of switched capacitor resistor  $R_3$ . In this condition, the PLL loop bandwidth is only determined by the choice of  $R_2$  and  $C_{\text{filter}}$  (resistor 424 and  
5 capacitor 422, respectively). In summary, using the switched capacitor resistance in the feed forward path allows the dynamic adjustment of loop bandwidth, which directly translates into improved transient response.

Figure 5 shows a simulation of normalized loop bandwidth  
10 versus frequency error. For the purposes of this simulation, the components were given the following values.

$$C_{\text{filter}} = 10\text{pF}, C = 1\text{pF}, R_2 = 10000 \text{ ohms}, \text{ and } R_{\text{onswitch}} = 1000 \text{ ohms}$$

15 Where  $C_{\text{filter}}$  is the capacitor in the LPF,  $C$  is the capacitor in the switched capacitor resistor, and  $R_{\text{onswitch}}$  is the ON resistance of the switch in the switch capacitor resistor.

It may be noted from FIGURE 5 that the loop bandwidth is  
20 increased by a factor of ten for a frequency error of 1GHz.

Turning now to FIGURE 6, a simplified version of R3 is illustrated. In FIGURES 4 and 6, the switched capacitor R3 is referenced with respect to  $V_{\text{ref}}$  rather than ground.  $V_{\text{ref}}$  is configured to have a lower potential than ground. Explanation  
25 for this will follow below.

In the discussion above,  $V_{\text{in}}$  is illustrated as quasi-stationary with respect to  $V_{\text{switch}}$ . It is the choice of  $V_{\text{ref}}$  that makes this argument valid.

Turning back to FIGURE 4 and referring to the  
30 characteristics with respect to frequency of the positive

terminal of resistor R2 (Node N) in FIG. 4, the voltage at Node N in FIG. 4 can be found using the following expression

$$V_n(s) = V_{pfd}(s) [R2 // R2] / [(R2 // R3) + 1/sC + R1]$$

5

Wherein  $V_n(s)$  is the voltage at Node N, and  $V_{pfd}(s)$  is the output of the PFD. In the above equation, low frequency signals are more attenuated than high frequency signals.

FIGURE 7 illustrates a typical plot of the frequency response at node n in FIGURE 4. In FIGURE 8, in one embodiment,  $V_{ref}$  and ground are at the same potential. Therefore, the characteristics for R3 of FIG. 8 can manifest. Note that when the frequency of  $V_{in}$  becomes comparable to or larger than that of  $V_{switch}$ ,  $I_{in\_average}$  is approximately equal to zero. In this case, the effective resistance provided by R3 is very large, and there is little modulation of PLL loop bandwidth.

FIGURE 9 illustrates characteristics when  $V_{ref}$  has a lower potential than ground. In FIG 9, a low frequency offset is introduced that dominates the high frequency ripple and makes  $V_{in}$  quasi-stationary with respect to  $V_{switch}$ . In FIG. 9,  $I_{in\_average}$  is greater than zero. As a result, the effective resistance of R3, and therefore the PLL loop bandwidth, can be modulated.

Although the invention has been described with reference to a specific embodiment, the description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiment, as well as alternative embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It is

therefore contemplated that the claims will cover any such modifications or embodiments that fall within the true scope and spirit of the invention.